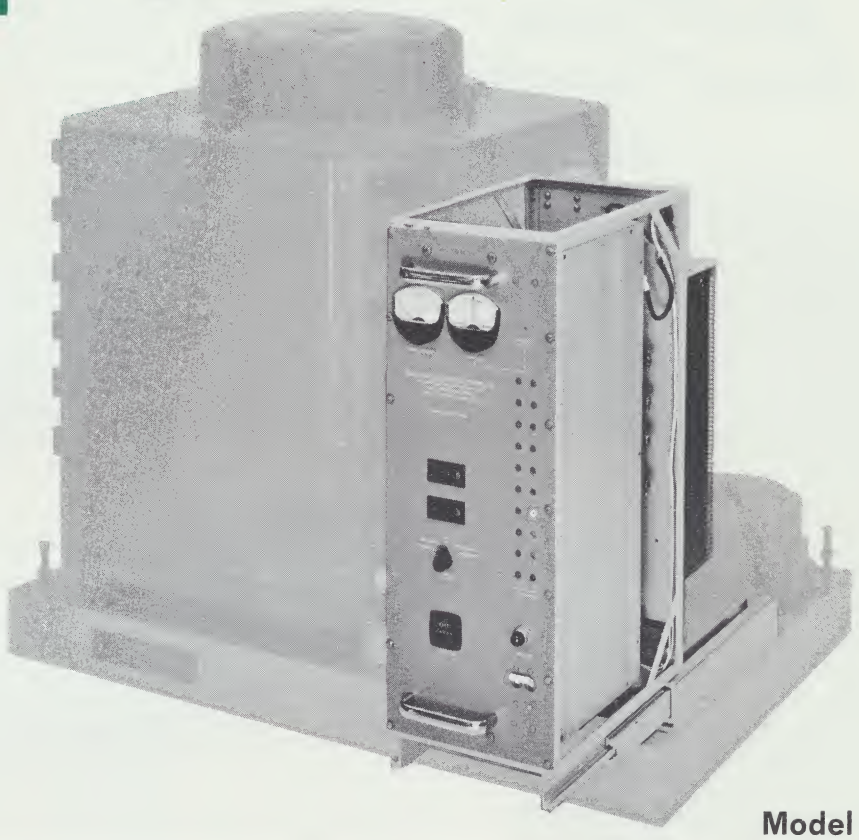
SEQUENTIAL ELECTRONIC SYSTEMS

MAGNETIC DRUM SYNCHRONIZATION SYSTEM



Model DS12

FEATURES

- Time displacement error less than 100 ns
- Unlimited number of drums can be electronically geared to perform as a single unit
- Non-volatile storage
- Absolute position control of all drums under all conditions i.e. even after power failure
- No trim adjustments
- Increases storage capacity of alpha-numeric display systems or digital computers on a modular basis
- Integrated circuit electronic assemblies available for airborne applications
- Projected electronics MTBF greater than 15,000 hours
- Meets all applicable MIL-SPECS

INTRODUCTION

The Sequential Magnetic Drum Synchronization System Model DS12 electronically gears any number of individual drums with a time displacement error (TDE) of less than 0.2 microseconds between any two arbitrary drums. Prior state-of-the-art required that a reference track on a single drum determine the clock rate of a digital computer or display system. Lack of precision drum synchronism, thereby restricted a computer or display to limited storage access obtainable by a single drum.

The technique employed by Sequential couples individual drums by means of an external reference frequency. This reference is utilized as the clock frequency for the computer or display system. Therefore, a flexible modular approach to present memory storage problems is now available. The storage capacity of a system can be increased, without limit, by the addition of any number of controlled drums.

OPERATION

The Sequential Drum Synchronization System Model DS12 may be described in terms of four (4) interacting control functions. These functions are:

a) The primary speed/phase control as implemented by an FPL SPEED/PHASE CONTROL LOOP.
b) A phase correction control as implemented by the PHASE CORRECTION LOOP.
c) A reference generator control as implemented by the REFERENCE GENERATOR LOOP.
d) An indexing control as implemented by the INDEXING LOOP.

Figure 2 is the System Block Diagram. This figure indicates the four (4) broad functional control loops. Figure 3 presents a functional block diagram of the system. In this block diagram each of the major blocks of Figure 1 have been broken down into several functional components.

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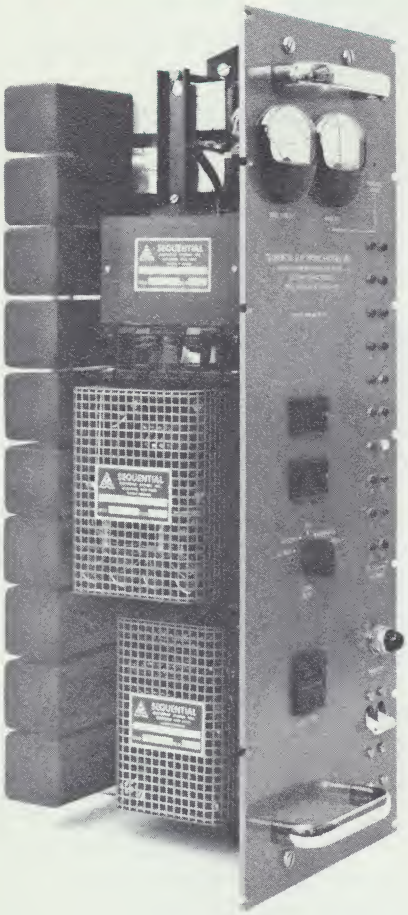


INPUT SIGNAL FUNCTIONS

A. *Reference Clock Signal*

The Reference Clock Signal is a timing pulse train whose leading edge generates incremental position commands to the drum, and whose frequency generates precise speed commands. The drum speed is directly proportional to the Reference Clock Signal frequency. If the Reference Clock Signal frequency is lowered, the drum will decrease in speed. If the Reference Clock signal frequency is increased, the drum will increase in speed.

B. *Reference Index Signal*

The Reference Index Signal is a command index pulse whose leading edge is aligned with a leading edge of one of the Reference Clock Signal pulses. The Index Signal repeats once per drum revolution. If the Reference Index Signal is removed, after the drum has achieved index synchronism, the drum will maintain index synchronism unless a disturbance occurs to shift the drum position by more than one bit spacing within the index slot.

C. *Drum Clock Signal*

The Drum Clock Signal is the high frequency (N pulses/rev) feedback control signal and is electromagnetically derived from a track on the drum.

D. *Drum Index Signal*

The Drum Index Signal is the once/rev feedback control signal and is electromagnetically derived from a track on the drum. This Index pulse is centrally located between two Drum Clock Signal pulses.

DUAL READ AMPLIFIER

The Dual Read Amplifier is used to shape and amplify the Drum Clock signal and the Drum Index signal. Figure 3 shows the input and output characteristics of the Dual Read Amplifier.

FPL SPEED/PHASE CONTROL LOOP

The Speed/Phase Control Loop utilizes as it inputs a reference pulse train that is generated by the Reference Generator Loop and the Phase Correction Loop, and a feedback pulse train that is derived from the Dual Read Amplifier.

This speed/phase loop locks the drum clock frequency to the incremental reference. The incremental reference and the drum clock signals are compared on a frequency/phase basis in the FPL* Computer Module which generates an error signal accordingly. The magnitude and polarity of the frequency error is such, that when converted to d.c., amplified, and passed to the brake driver, the drum is forced to rotate at a speed at which the clock pulse frequency equals the reference frequency.

To maintain precise synchronization, a phase error signal is generated once the drum has achieved synchronism. The phase error signal controls the brake excitation to maintain "tight" phase alignment between the reference pulse train and the feedback signal, when frequency-lock has been achieved.

The unique feature of the FPL Computer is that the frequency lock and phase lock logic operate simultaneously, and the transition from the frequency control mode to the phase control mode is automatically performed in a continuous manner, so that no switching signals or transients appear in the error signal.

The phase error information produced by the computer is in the form of relative pulse spacing between the reference and tachometer signals.

The function of the D/A CONVERTER MODULE is to convert the above relative pulse spacing (phase error) information into a d.c. signal proportional to the phase error. This conversion is performed on a pulse-to-pulse basis, with no significant time constant, and with virtually no ripple. The electrical bandwidth is one-half the frequency of the reference signal, which permits design of an extremely wideband and high gain control loop.

The STABILIZATION MODULE contains circuitry which applies phase, velocity, and acceleration control in the proper ratio, and with proper frequency characteristics, so as to optimize the closed loop performance of the control loop. This module also contains circuitry associated with the Brake Driver Assembly.

The BRAKE DRIVER ASSEMBLY supplies correct excitation to the Brake windings to maintain precise drum synchronism. Excitation signals from the Driver are fed back to the Stabilization Module, so that the driver and brake windings are operated in a secondary closed loop manner. The effect of this type of operation is to linearize the torque output characteristics, and to virtually eliminate the electrical inductive time constant of the brake windings.

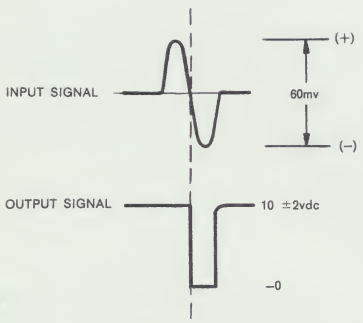


Figure 1 – Dual Read Amplifier Signal Characteristics

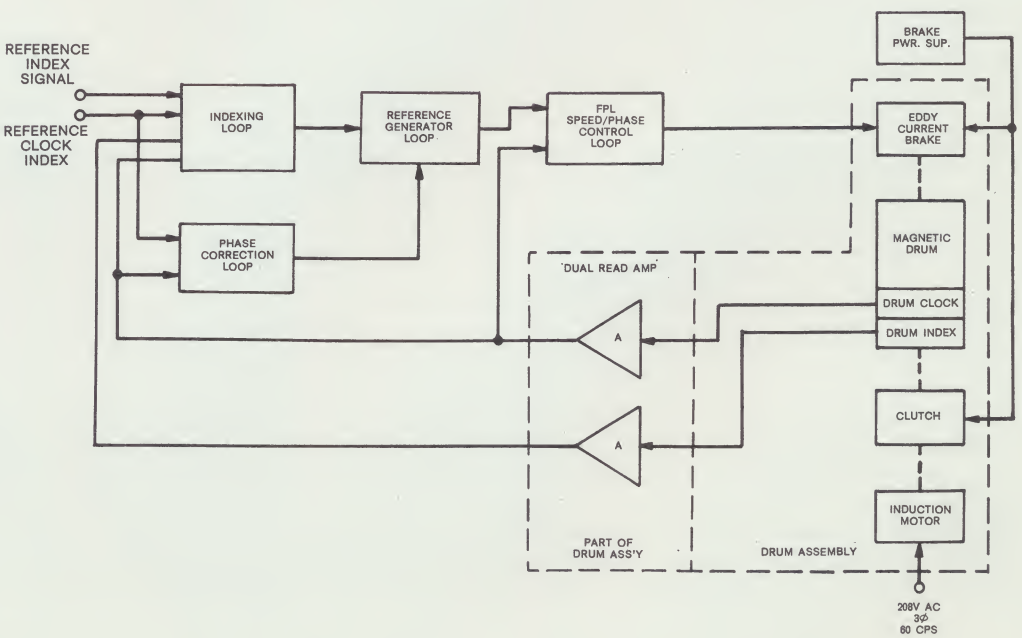
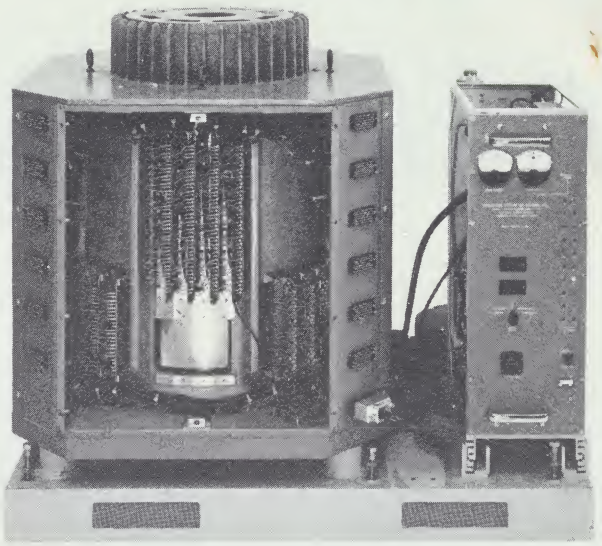


Figure 2 – System Block Diagram: Sequential MDSS* Control and Indexing System Model No. DS12

SEQUENTIAL MAGNETIC DRUM SYNCHRONIZATION SYSTEM

MODEL DS12



SPECIFICATIONS

Drum Speed (ΩRPM)	Specified by customer
Drum Clock Pulse Density (N)	Based on Specific application
Reference Signals	
Clock Signal	
Frequency	$f = \frac{\Omega N}{60}$ cps
Waveform	Zero Based Position Pulse
Amplitude	2 volts
Base line noise	±0.15 volts max
Duty Cycle	less than 50%
Rise Time	0.15 microseconds max
Source Impedance	600 ohms max
Index Signal	
Frequency	$f = \frac{\Omega}{60}$ cps
Waveform	Zero based positive pulse
Amplitude	2 volts
Base line noise	±0.15 volts max
Duty cycle	less than 50%
Rise time	0.15 microseconds max
Source Impedance	600 ohms max
Phase Alignment	Reference Index Pulse must be phase locked (counted down from the clock signal) to the clock signal and aligned with a clock pulse within ±0.5 microseconds
Drum Signals	
Clock Signal	
Frequency	$f = \frac{\Omega N}{60}$ cps
Waveform	essentially sinusoidal pulse
Amplitude	60 mv p-p min
Signal Source	Magnetic Head
Signal-to-Noise Ratio	12 db min
Index Signal	
Frequency	$f = \frac{\Omega}{60}$ cps
Waveform	essentially sinusoidal pulse
Amplitude	60 mv p-p min
Signal Source	Magnetic Head
Signal-to-Noise ratio	12 db min
Phase Alignment	Drum Index Pulse to be located approximately 180 degrees between two clock pulses
Absolute Position Accuracy (Time Displacement Error, TDE)	±0.1 microseconds non cumulative
Input Power	
Voltage	115 volts single phase or 208 volts 3 phase
Frequency	60 cps or 400 cps
Current	Based on specific application
Size	
Electronic Control Console (1)	9″ w x 24″ h x 11″ d
Brake Power Supply	Based on specific application
Dual Read Amplifier	3″ w x 3″ h x ¾″ d
Temperature Range	
Operating	0°C to +60°C
Non-operating	−55°C to +71°C
Humidity	97%
Vibration	.005 inches double amplitude from 10 to 55 cps; .005 inches double amplitude from 55-500 cps with a maximum acceleration of 5 g's
Shock	5 g's in any plane, 11 milliseconds duration

Note

1. Miniaturized integrated circuit electronic assembly available

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